

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 6,941,415 B1
APPLICATION NO. : 09/641519
DATED : September 6, 2005
INVENTOR(S) : Kevin J. Ryan

Page 1 of 9

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Title page should be deleted and substitute therefore the attached title page as shown on the attached page.

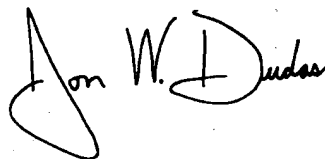
Drawings:

Delete drawing sheets 1-7, and substitute therefore the drawing sheets, consisting of Figs. 1-7, as shown on the attached pages.

Claim 20, column 9, line 30, "Link" should read --link--.

Signed and Sealed this

Tenth Day of October, 2006

A handwritten signature in black ink, reading "Jon W. Dudas". The signature is stylized, with a large, looped initial "J" and a distinct "D".

JON W. DUDAS
Director of the United States Patent and Trademark Office



US006941415B1

(12) **United States Patent**
Ryan

(10) Patent No.: **US 6,941,415 B1**
(45) Date of Patent: **Sep. 6, 2005**

(54) **DRAM WITH HIDDEN REFRESH**

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(73) Assignee: Micron Technology, Inc., Boise, ID (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 274 days.

(21) Appl. No.: 09/641,519

(22) Filed: Aug. 21, 2000

(51) Int. Cl.⁷ G06F 12/00

(52) U.S. Cl. 711/106; 711/167; 711/168

(58) Field of Search 711/104, 105, 711/100, 167, 168; 305/222, 189.01, 200, 193

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(57) **ABSTRACT**

A synchronous DRAM is provided having specified time slots (e.g., every multiple of 4 clock pulses of a DRAM input clock) within which read or write commands may be entered on the command/address bus. During operation, the DRAM performs internally generated refresh operations on a periodic basis while avoiding collisions with controller-generated data accesses. An internal refresh cycle can be executed without interfering with any data accesses by starting the refresh after decoding a non-conflicting command in one of these time slots and finishing before the next command time slot. If an internal refresh operation is delayed (e.g., by the decoding of a conflicting access command) it will be completed at the earliest opportunity thereafter.

37 Claims, 7 Drawing Sheets

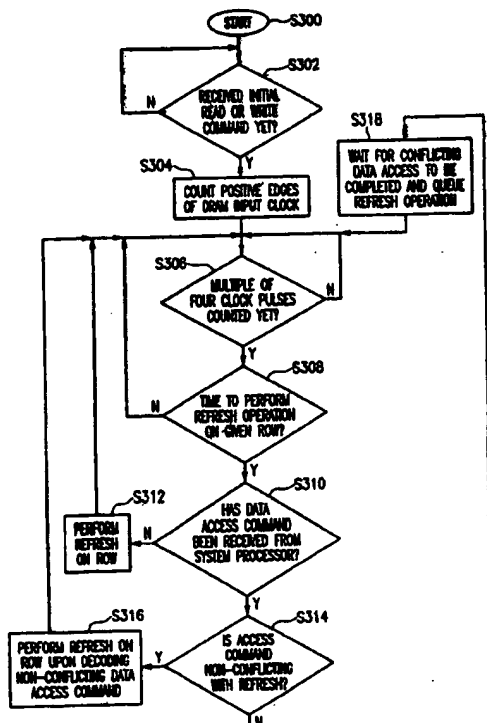




FIG. 1



FIG. 2

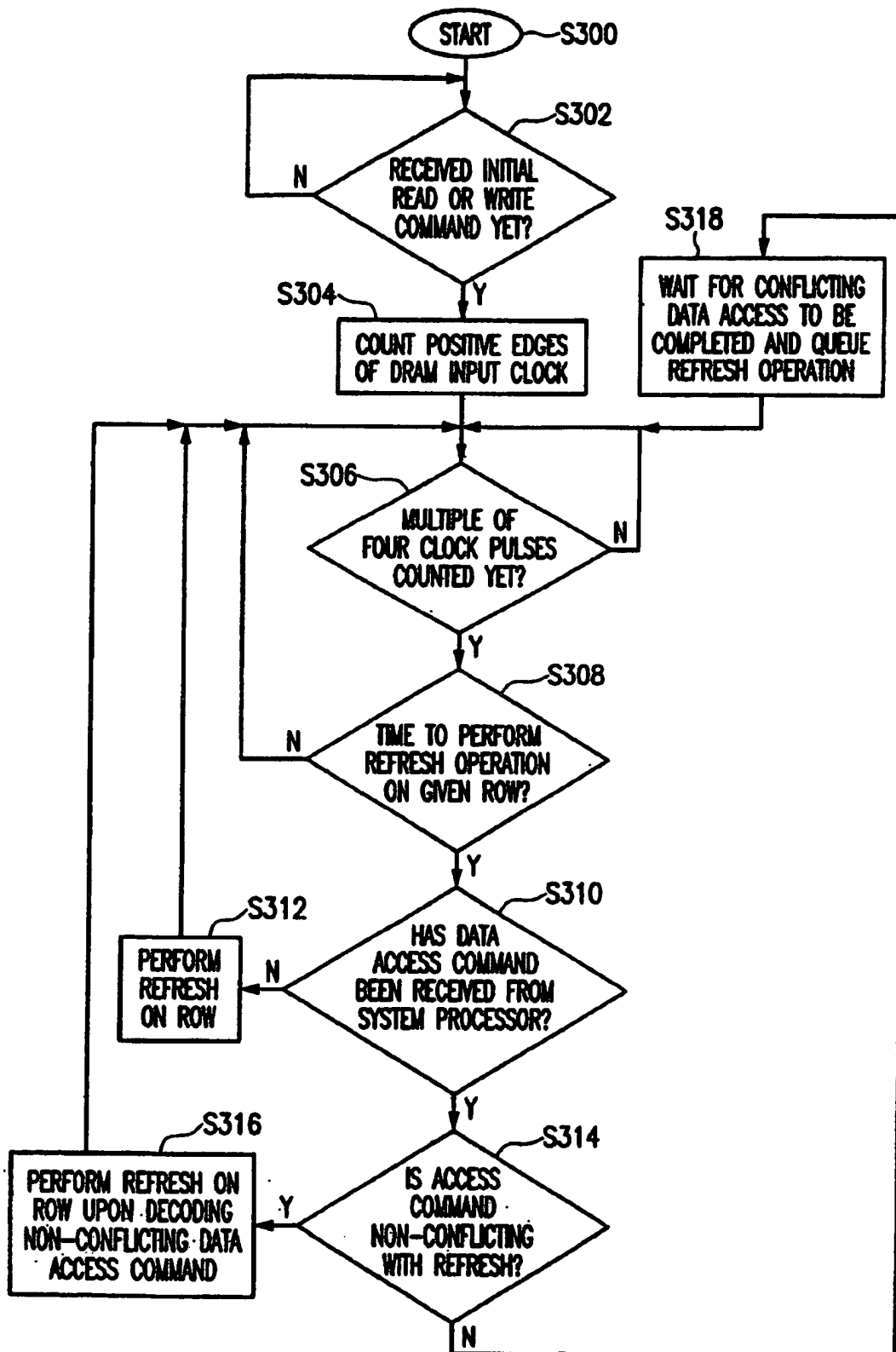


FIG. 3

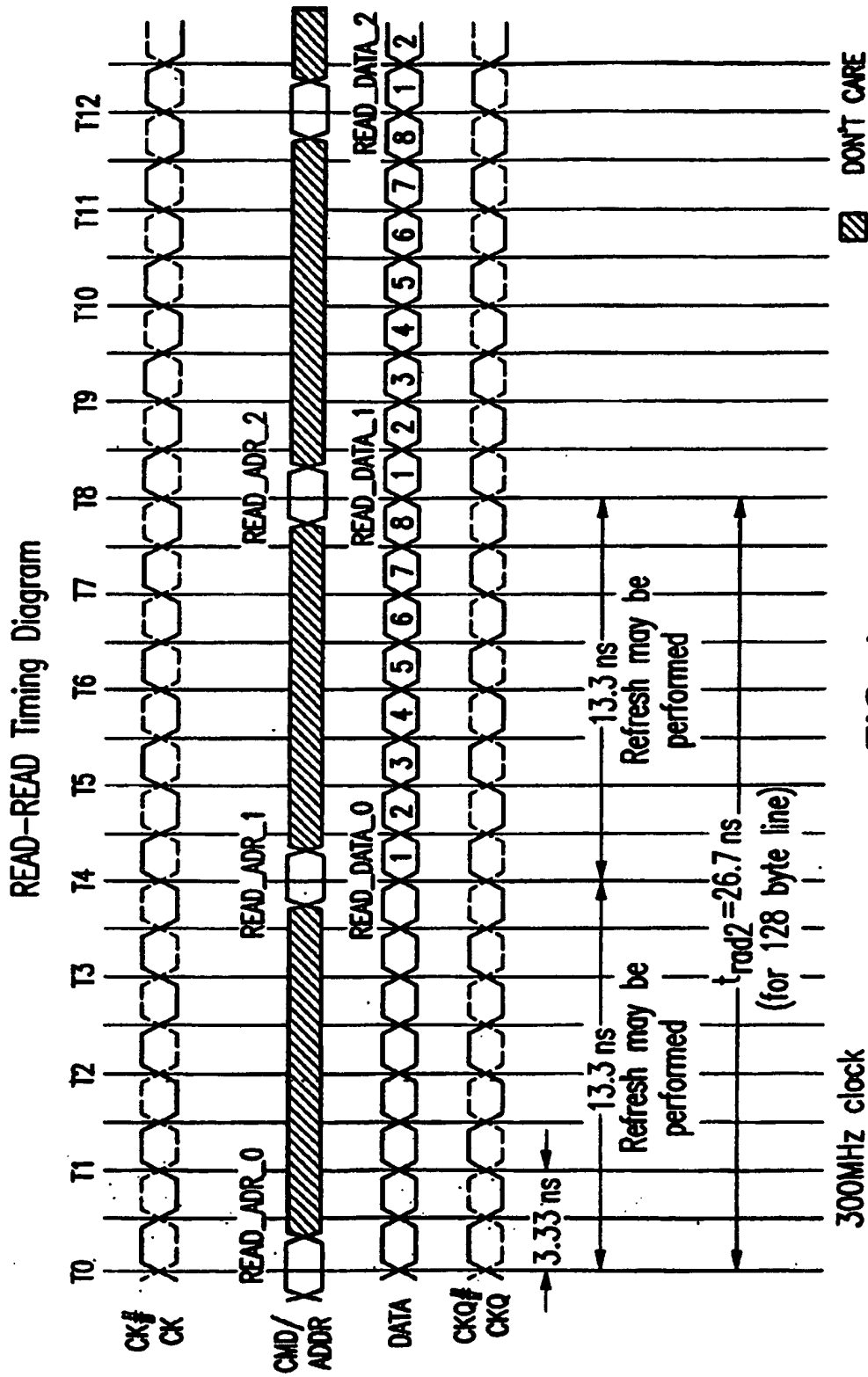


FIG. 4

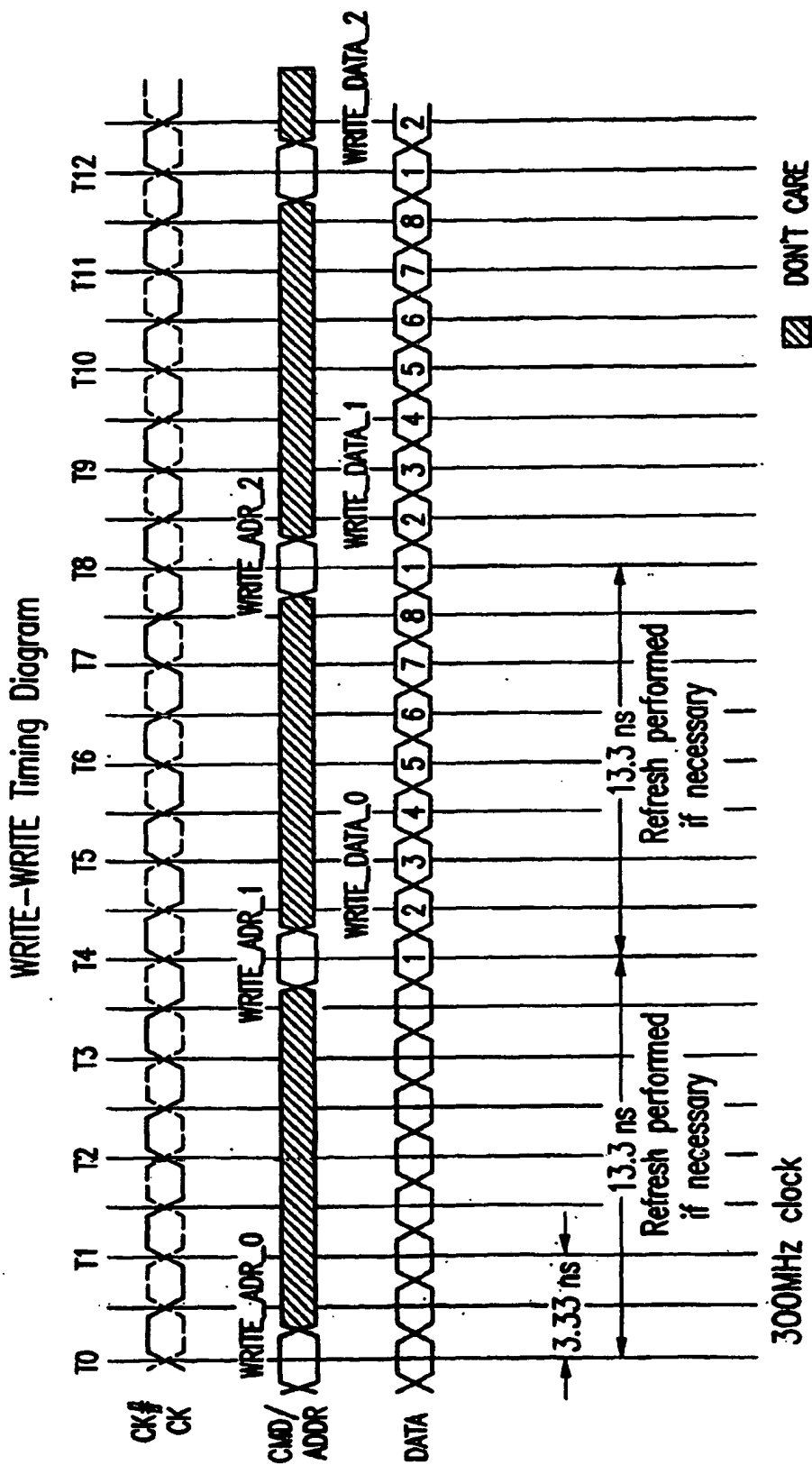


FIG. 5

300MHz clock

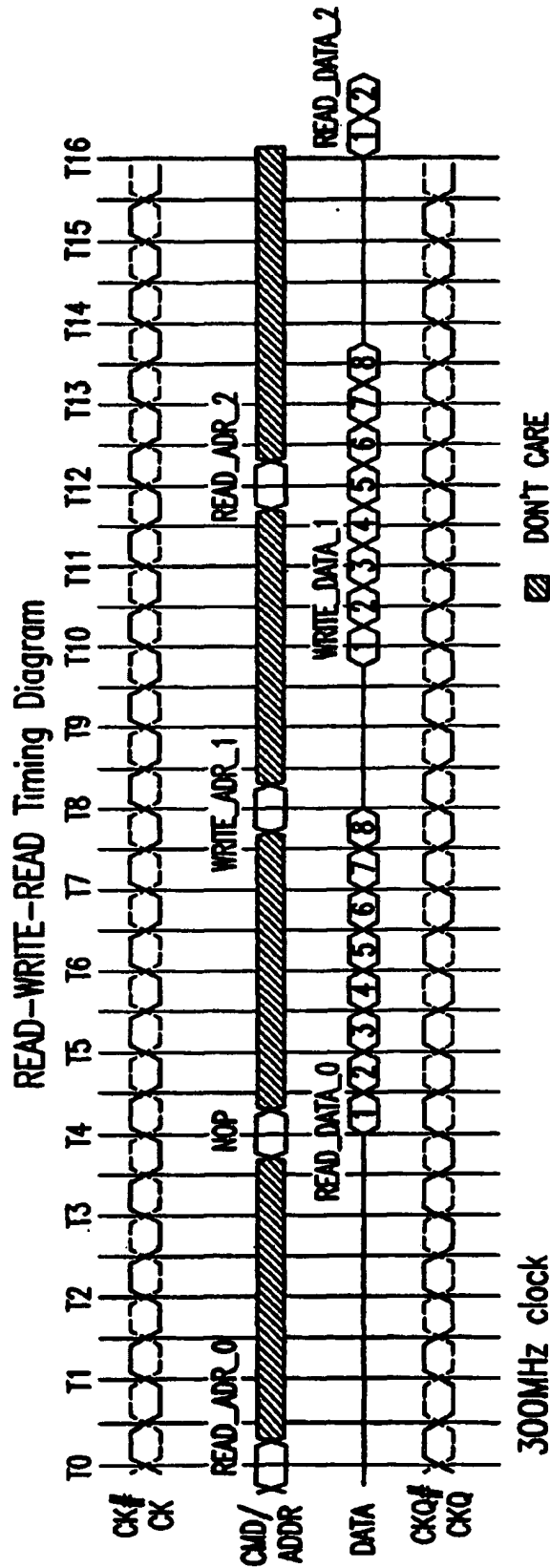


FIG. 6

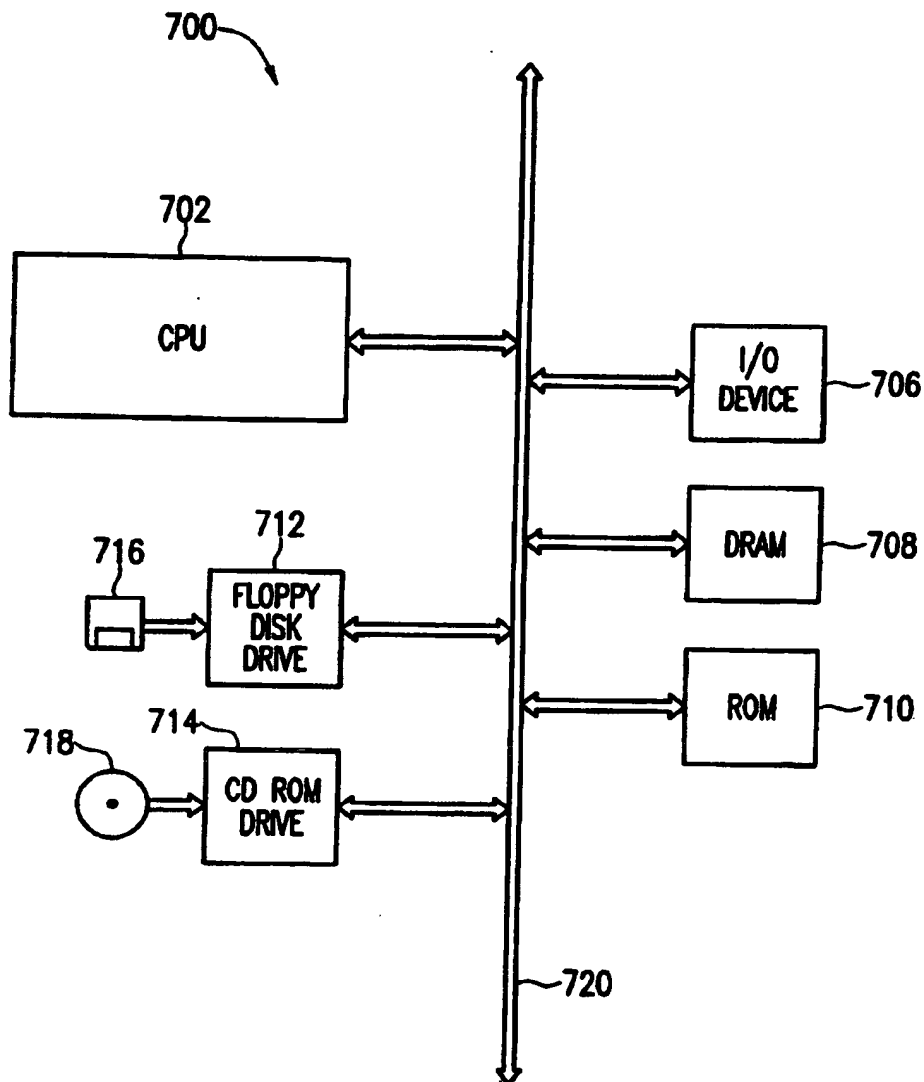


FIG. 7